REFERENCES

[1] T. Tanaka, K. Tsunoda, and M. Aikawa, "Slot-coupled directional couplers between double-sided substrate microstrip lines and their applications," *IEEE Trans. Microwave Theory Tech.*, vol. 36, pp. 1752–1757, Dec. 1988.

[2] N. Herscovici and D. M. Pozar, "Full-wave analysis of aperture-coupled microstrip lines," *IEEE Trans. Microwave Theory Tech.*, vol. 39, pp. 1108–1114, July 1991.

[3] M. F. Wong, V. F. Hanna, O. Picon, and H. Baudrand, "Analysis and design of slot-coupled directional couplers between double-sided substrate microstrip lines," *IEEE Trans. Microwave Theory Tech.*, vol. 39, pp. 2123–2129, Dec. 1991.

[4] C. Wan, "Quasistatic analysis of slot-coupled double-sided microstrip lines by conformal mapping," *Microwave Opt. Technol. Lett.*, vol. 9, pp. 253–256, Aug. 5, 1995.

[5] R. B. Tsai and K. L. Wong, "Characterization of cylindrical microstriplines mounted inside a ground cylindrical surface," *IEEE Trans. Microwave Theory Tech.*, vol. 43, pp. 1607–1610, July 1995.

[6] ——, "Quasistatic solution of a cylindrical microstripline mounted inside a ground cylinder," *Microwave Opt. Technol. Lett.*, vol. 8, pp. 136–138, Feb. 20, 1995.

[7] N. G. Alexopoulos and A. Nakatani, "Cylindrical substrate microstrip line characterization," *IEEE Trans. Microwave Theory Tech.*, vol. 35, pp. 843–849, Sept. 1987.

[8] R. B. Tsai, "Analysis of cylindrical printed slot and slot-coupled microstrip antennas," Ph.D. dissertation, Dept. of Electrical Eng., National Sun Yat-Sen Univ., Kaohsiung, Taiwan, June 1995.

Substrate Parasitics and Dual-Resistivity Substrates

Rex Lowther, Patrick A. Begley, George Bajor,
Anthony Rivoli, and William R. Eisenstadt

***Abstract*—In high-frequency semiconductor applications, substrate effects can be a dominant source of parasitics unless they are carefully minimized. Here a dual-resistivity substrate in a bonded-oxide process is considered for the optimization of the two major types of substrate parasitics: resistive substrate losses and capacitive coupling (crosstalk) through the substrate. These will both depend on the frequency, the two substrate resistivities, and the thickness of the two substrate layers. The thickness of the upper layer is treated as a fully designable parameter. The mechanisms will be evaluated numerically, but intuitive rule-of-thumb arguments will also be provided for a good understanding of the physics and of the tradeoffs in selecting an optimal design. The results of these sections may also serve as a guide for determining standard substrate resistivities.**

I. INTRODUCTION

Integrated circuits that operate at microwave frequencies are implemented on substrates comprising monocrystalline gallium arsenide or by using hybrid circuit techniques. These technologies are effective in producing integrated circuits operating at microwave frequencies, but they still have several drawbacks. Both technologies can be expensive and generally produce circuits of low device density compared to the cost and density of devices in planar silicon integrated circuits. Attempts to implement microwave frequency integrated circuits with conventional silicon technology have been limited due to high losses occurring in the silicon substrate at gigahertz frequencies [1]. These lossses lower transistor performance and also greatly lower the Q factor of integrated silicon inductors and capacitors. Highly resistive float-zone silicon substrates (HRS), however, have been shown to limit these losses nearly as well as GaAs and these have also been successfully applied at multigigahertz frequencies [1]–[5]. Unfortunately, these substrates are very expensive and are limited in wafer diameter to 100 mm. A dual-substrate structure, analyzed herein, describes a bonded-wafer process that has resistive substrate losses nearly as low as HRS, and lower cross-talk than HRS—while retaining the much lower cost of conventional bonded wafers.

Manuscript received August 28, 1995; revised March 20, 1996.

R. Lowther, P. A. Begley, G. Bajor, and A. Rivoli are with Harris Semiconductor, Melbourne, FL USA.

W. R. Eisenstadt is in the Department of Electrical Engineering and Computer Science, University of Florida, Gainesville, FL USA.

Publisher Item Identifier S 0018-9480(96)04726-6.

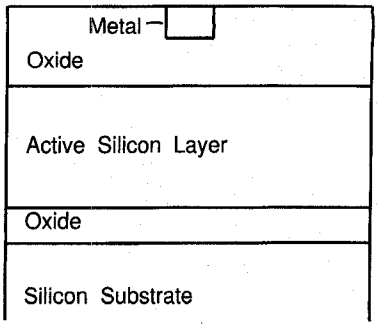


Fig. 1. Cross-section of a typical SOI geometry.

In the next section, resistive losses from induced current are analyzed and estimated for both standard and dual-resistivity substrates. The simple, but illustrative, and worst-case example of a long, straight metal line is used to get an estimate of these losses. The two following sections analyze capacitive coupling of nearby devices through the substrate for both standard substrates and the proposed dual substrates, respectively. Finite-difference device simulation is used to obtain an understanding of, and estimates of, the cross-talk. In the "process" section, the most likely method for making such a structure is discussed. Finally, design examples are chosen to illustrate the tradeoffs in the substrate parameters, and the comparative value of the dual-resistivity substrate structure to standard highly resistive substrates is discussed.

II. SUBSTRATE RESISTIVE LOSSES

Consider first the worst-case example of a very long, straight metal line running over various layers as shown in cross section in Fig. 1. In nearly all practical cases, induced current in the active silicon layer can be ignored because it is thin compared with its own skin depth for most typical doping levels and because areas of high doping are usually confined, isolated regions too small to allow significant conduction. The active silicon region therefore can be considered to be an insulator for this parasitic—allowing the device layer and the two oxide layers in Fig. 1 to be treated as a single insulator.

Assume for now a uniform substrate with resistivity low enough that the skin depth is much less than the substrate thickness. For distances more than a few skin depths below the substrate-insulator interface, it is known that both the electric and magnetic fields due to ac current are essentially zero. Therefore the sum effect of the induced electric field is to generate current such that it is equal in magnitude and opposite in direction to the ac current in the metal line. This is simply return current in a ground plane. At microwave

frequencies, as will be shown, these induced resistive losses can be greater than those in the metal lines.

For the substrate resistivities considered here ($\rho \leq 0.02\ \Omega$–cm), it can be assumed that the induced current is locally in phase with the electric field E for frequencies up to 100 GHz (and higher). This allows us to drop the displacement current term, and the solution of Maxwell's equations for the electric field then becomes

$$\nabla^2 E - j\omega\mu E/\rho = 0. \tag{1}$$

The goal here is to derive a rough, quick estimate for induced substrate resistance. Along these lines, consider Fig. 1 such that the entire structure is conformed into cylindrical symmetry about an axis centered on the metal line. This approximation will be justified later in this section. Switching to cylindrical coordinates, (1) transforms to

$$\frac{1}{r}\frac{d}{dr}\left(r\frac{dE_z}{dr}\right) - 2jE_z/\delta^2 = 0 \tag{2}$$

where δ is the skin depth

$$\delta = \left(\frac{2\rho}{\mu\omega}\right)^{1/2}. \tag{3}$$

E_z is the component of the electric field E in the axial direction, ω is the angular frequency, μ is the magnetic permeability, ρ is the resistivity of the substrate, and r is the distance to the center of the metal line. The solutions to (2) are Bessel functions of complex arguments. The correct combination of these Bessel functions was determined by applying the boundary conditions that the electric and transient magnetic fields are zero at large r. The latter was done by forcing the integrated electric field (or current density) to be equal in magnitude and opposite in phase to the current in the metal line. From this solution, the integral of EE^*/ρ was performed to get the resistive power loss in the substrate. Since the current is fixed for low resistivities, this power loss is proportional to the substrate resistance. In fact, the substrate resistance R can be defined by this relationship. This exact numerical result for R is easily approximated by the simple analytic formula

$$R_{\text{analytic}} = \frac{\rho l}{\pi(d+\delta)^2 - \pi d^2} = \frac{\rho l}{\pi\left[d + \left(\frac{2\rho}{\mu\omega}\right)^{1/2}\right]^2 - \pi d^2} \tag{4}$$

where l is the length of the metal line and d is the distance from the metal line to the "inner" edge of the substrate. The denominator in (4) is the area of a δ-wide strip at the inner surface of the substrate. This formula overestimates the Bessel function formula for R by a factor of 1.27 in the limit of large δ and, as expected, approaches this result when the substrate distance is large compared to the skin depth, and the physics becomes more locally planar. From (4), it is shown that, for $d \ll \delta$, R is proportional to the frequency and independent of the resistivity! For $d \gg \delta$ the more familiar relationship is obtained—that R is proportional to the square root of both frequency and resistivity.

Qualitatively, all these effects will still be present for the actual, planar geometry. The main difference is that the available area for conduction is decreased. After examining the structures, R was increased by a factor of two over the cylindrical result to account for this difference. Equation (4) can also be modified to include a finite width w of the metal line in parallel with the above solution. With these two rough refinements, the formula for substrate resistance becomes

$$R_{\text{analytic}} = \frac{\rho l}{\pi(d+\delta)^2/2 - \pi d^2/2 + w\delta}$$

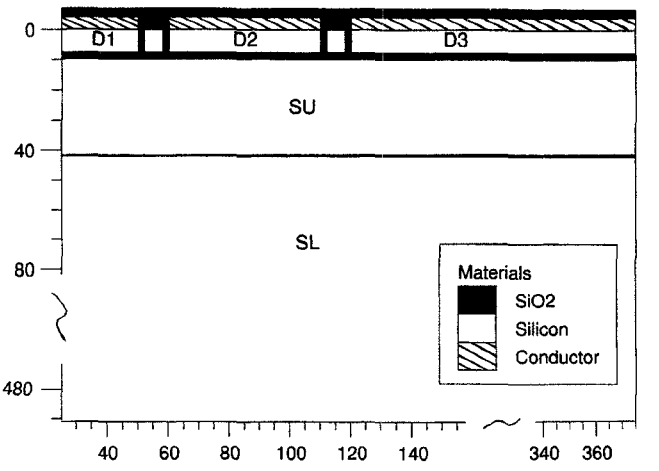


Fig. 2. Three adjacent idealized devices isolated by trench and by a bottom oxide. AC bias is applied to D1. Symmetry about the left side of this structure is assumed. The substrate may be divided into upper and lower regions (S_U and S_L) with different doping levels.

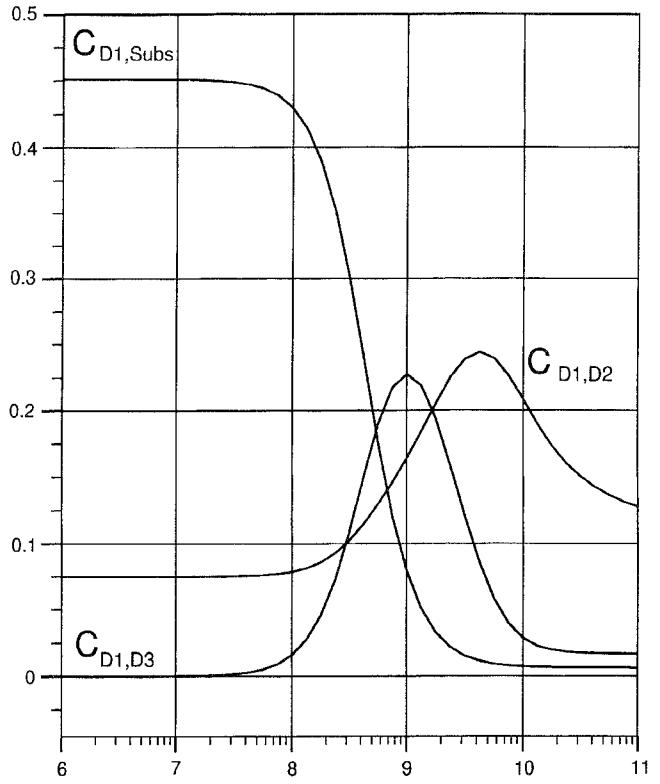
$$= \frac{\rho l}{\pi\left[d + \left(\frac{2\rho}{\mu\omega}\right)^{1/2}\right]^2 \Big/ 2 - \pi d^2/2 + w\left(\frac{2\rho}{\mu\omega}\right)^{1/2}}. \tag{5}$$

To minimize R, (5) shows that it is desirable to make d large and to make the resistivity of the substrate as low as possible. Typically this has not been done because the substrate distances range around 10 μm or less. With standard SOI, d can't be increased by increasing the bottom oxide thickness due to the high thermal resistance of the oxide. The advantage of HRS is that the skin depth is large compared to the substrate thickness, and essentially no current flows in the substrate. In this case the silicon can be considered as the insulator, and the distance to the substrate d can be replaced by the distance to the metal upon which the silicon sits.

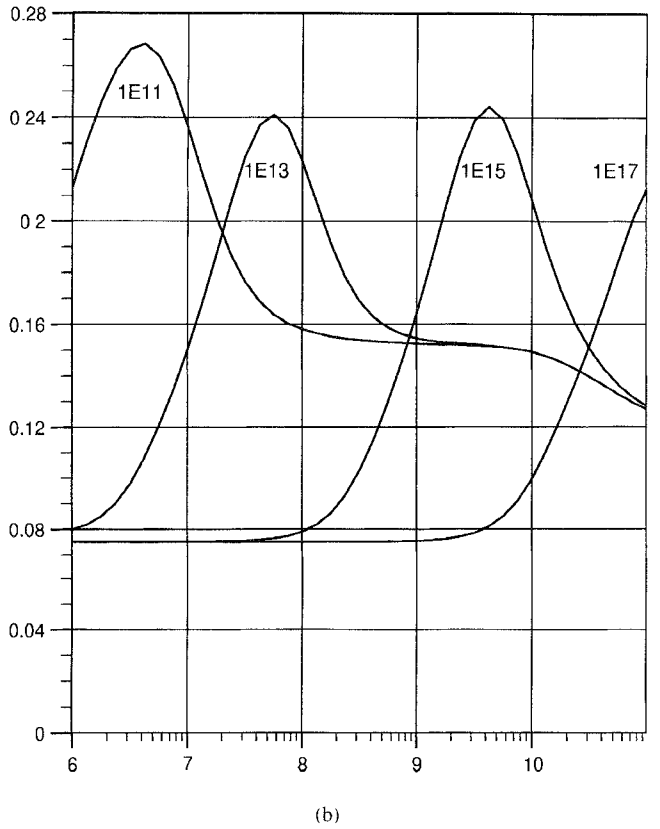
III. Cross-Talk, Standard Substrates

Substrates also act as parasitic capacitors coupling nearby devices. Fig. 2 shows an example structure containing three nearby analog devices $\{D1, D2, D3\}$ with total lengths of 46 μm, 46 μm, and 280 μm, respectively. Results from numerical device simulation (Atlas [6]) are shown in Fig. 3(a) by plotting elements from the capacitance matrix $\{C_{D1,D2}, C_{D1,D3}, C_{D1,Sub}\}$ against frequency. The substrate doping in this case is uniform at 10^{15} cm^{-3}. Most of the field lines initiated in $D1$ are terminated at the top of the substrate below, while most of the rest travel directly to $D2$. At low frequencies, all of this substrate charge can be supplied by the substrate contact because the charging time (or RC constant) is small compared to the time of oscillation. But as the frequency increases, this path gets "frozen out" as the oscillation time becomes small wrt. RC. As this happens the less resistive couplings from nearby devices now compete to supply this charge. At the intermediate frequency of 10^9 Hz, the capacitive coupling $C_{D1,D3}$ is actually greater than $C_{D1,D2}$ because $D3$—meant to represent a collection of nearby devices—has a much larger surface exposed to the substrate than $D2$. As the frequency is increased further, however $C_{D1,D3}$ drops almost to zero while $C_{D1,D2}$ dominates because it has a much lower path resistance.

Fig. 3(b) and (c) shows $C_{D1,D2}$ and $C_{D1,D3}$, respectively, each over a range of uniform substrate dopings $\{10^{11}, 10^{13}, 10^{15}, 10^{17}\}$ cm^{-3}. In general, the trends are the same, but shifted toward the higher frequencies for the more highly doped substrates. At low

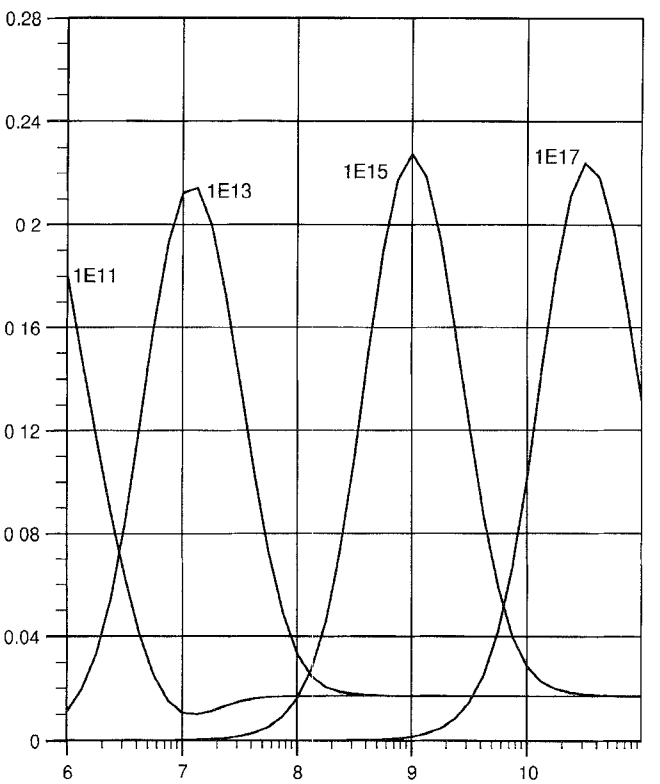


(a)



(b)

Fig. 3 (a) The D1 column of the capacitance matrix $\{C_{D1,Subs}, C_{D1,D2}, C_{D1,D3}\}$ on a standard substrate is plotted in fF/μm against $\log_{10}$ (Frequency) as applied to D1. (b) $C_{D1,D2}$ for the substrate doping concentrations $\{10^{11}, 10^{13}, 10^{15}, 10^{17}\}$ cm^{-3}.



(c)

Fig. 3. *(Continued)* (c) $C_{D1,D3}$ for the substrate doping concentrations $\{10^{11}, 10^{13}, 10^{15}, 10^{17}\}$ cm^{-3}.

frequencies, $C_{D1,D2}$ is dominated by the direct dielectric capacitance from fields above the substrate; at higher frequencies—in the peaks of Fig. 3(b) (as the substrate coupling freezes out)—the conductive path through the substrate allows additional coupling between $D1$ and $D2$; at even higher frequencies, this conductive path also freezes out—leaving in its place the dielectric coupling, including fringing through the substrate that was shielded at low frequencies. From Fig. 3(c), it is apparent that these effects are present for second nearest neighbors but are much different in magnitude. At frequencies above and below the peak, $C_{D1,D3}$ drops nearly to zero.

IV. Cross-Talk, Dual-Resistivity Substrate

The above analysis is now repeated for the same devices, but with a substrate that is divided into two layers. The upper layer of the substrate, S_U, should have a higher resistivity than the lower layer, S_L. In this example, S_U is 30 μm thick and is doped at $\{10^{11}, 10^{13}, 10^{15}, 10^{17}\}$ cm^{-3}, while S_L is generally doped as high as possible -10^{20} cm^{-3} in this example.

Corresponding to Fig. 3(b) and (c), Fig. 4 shows both $C_{D1,D2}$ and $C_{D1,D3}$ for these dual substrate devices. The peak of $C_{D1,D2}$ is significantly reduced from the uniform substrate result, while $C_{D1,D3}$ is reduced by better than a factor of 10. For a physical understanding of this, consider the path of the ac current from $D1$ to $D3$ to be divided into two parts: Path 1 is defined as entirely through the upper, more highly resistive part of the substrate S_U, while Path 2 is down through S_U from $D1$, lateral through S_L, and finally up through S_U to $D3$. As before, at low frequencies, $C_{D1,Sub}$ dominates and shields any substrate coupling between devices. But as the frequency is increased, resistive substrate current freezes out due to resistance in the upper part of the substrate (leaving only displacement current in this region). During this transitition, however, resistive current

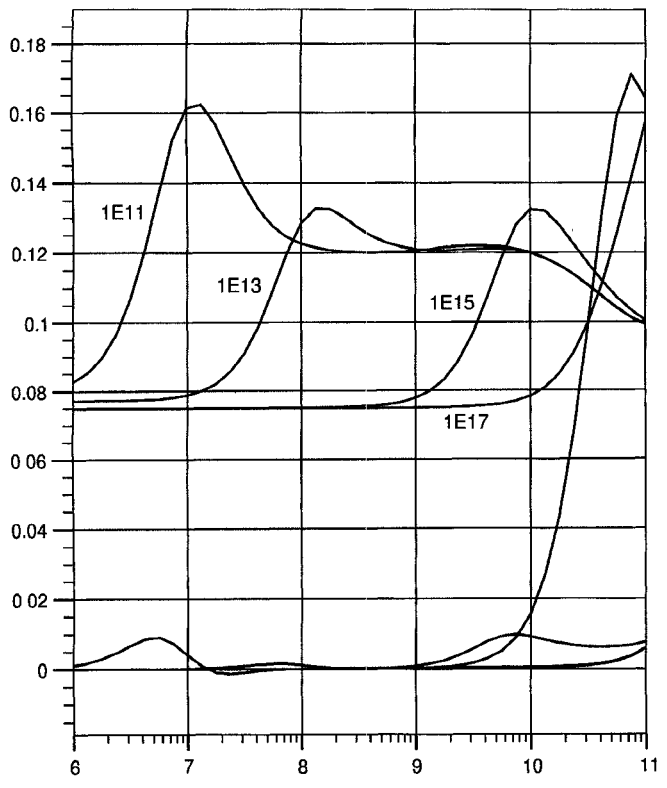


Fig. 4. $C_{D1,D2}$ and $C_{D1,D3}$ are plotted in fF/μm against $\log_{10}$ (Frequency) for the dual-resistivity substrate device. The upper substrate doping concentrations shown are $\{10^{11}, 10^{13}, 10^{15}, 10^{17}\}$ cm^{-3}.

through Path 2 has already begun to freeze out because it has a resistance approximately double that for current from the substrate (which only passes through S_U once). Similarly, since the thickness of S_U was chosen to be about the same or less than the device widths, resistance through Path 1 is also greater than resistance to the substrate by at least the same amount. At frequencies higher than this transition, ac current through the upper substrate between neighboring devices is primarily displacement current. Note, however, that cross-talk from displacement current is also reduced by the shielding of S_L. Displacement current through Path 1 must still compete with charge supplied by the substrate. More importantly, any displacement current to or from S_L (as in Path 2) gets intercepted by the highly doped region S_L, which is still controlled by the substrate contact.

For devices or metal lines for which capacitive cross-talk is a particular concern, the dual substrate structure provides a definite guideline during layout: By spacing the devices by a couple multiples of the S_U thickness, cross-talk is virtually eliminated. In the example used here, this is demonstrated by the differences in $C_{D1,D2}$ and $C_{D1,D3}$ for the dual substrate as shown in Fig. 4. Even without $D2$ to provide additional shielding, a separate simulation shows that $C_{D1,D3}$ is still smaller than the $C_{D1,D2}$ of Fig. 3(b) by about a factor of 10. For standard substrates, there is only a slow roll-off with distance.

V. Process

One possible way of making a dual-resistivity substrate is to start with a highly doped N-type (either antimony or arsenic) handle wafer. On this substrate is deposited a thin layer of undoped epi to act as a diffusion barrier to prevent dopants from migrating upward from the heavily doped substrate. Following the epi layer, a thick layer of undoped (as much as possible) polysilicon is deposited. According to [7] this should be enough to make the poly-Si highly resistive. Alternatively, and if necessary, a small amount of oxygen can be added to the poly either to make a highly resistive SIPOS layer or to act as a diffusion barrier. From this point, typical BESOI processing steps are applied.

VI. Design Examples

Suppose we have a circuit to perform at 10 GHz. We also want substrate resistances to be about equal to or less than that of the widest metal lines used in the layout (say 10 μm wide and 1.5 μm thick in this example, or about 33 Ω/cm). Assuming the resistivity of S_U is high enough such that its skin depth is very high wrt. its own thickness, then d in (5) is the distance between the metal line and the S_U/S_L interface. Using (5), $d = 40$ μm (corresponding to the thickness of 30 for S_U in the above example), and assuming a resistivity of 4×10^{-4} Ω-cm (a doping of 2×10^{20} cm^{-3}) for S_L, the total substrate resistance comes to 28 Ω/cm—less than that of the metal line. In addition to the tolerably low substrate losses, the cross-talk advantages of the dual-resistivity substrate are as described in the previous section. The S_U doping (or resisitivity) can now be chosen for the optimum capacitance profiles. From Fig. 4, any value from 10^{15} cm^{-3} or below (resistivity of 0.4 Ω-cm or higher) should be acceptable.

For smaller devices, the S_U thickness must also be smaller to provide the same shielding as in the above example. Otherwise the charge on $D1$ will be primarily neutralized by charge flowing from $D2$ rather than from the substrate. This will increase the substrate resistance, yet this may still be acceptable for most designs. In this case, if the S_U thickness is reduced to 15 μm, then $d = 25$ μm and the substrate resistance is 42 Ω/cm at 10 GHz—more than that of the last example but sill comparable to that of the metal line.

The final decision on the S_U thickness should be determined by the devices that need to be shielded from cross-talk and how closely packed they are. If this distance can be made greater than roughly one time the S_U thickness, then cross-talk will be very small. If this is not possible, and the devices must be adjacent, then any residual cross-talk through the substrate can still be mininized by choosing the highly resistive S_U case so that the peak capacitance occurs below the lowest operating frequency (see Fig. 4).

VII. Conclusion

Physically based estimates of substrate resistance and cross-talk were developed. These can be used as guidelines for optimizing substrate properties for the minimization and trade-off of these parasitics. A dual-resistivity substrate is described and is shown to have less cross-talk than standard HRS. Fig. 3(b) and (c) show that even the most highly resistive substrates still allow significant cross-talk at 1 MHz, and for most circuits that have components at 10 GHz there are often other parts of the circuit running at lower frequencies where cross-talk can be important.

The dual-resistivity substrate of the last example provided a good tradeoff between cross-talk and substrate resistive losses at 10 GHz. At lower frequencies, the tradeoffs are much easier. The lower value of R allows for a thinner S_U, and therefore greater shielding by S_L. At frequencies much higher than 10 GHz, exotic structures such as an embedded silicide layer or a very thin substrate on metal will be necessary to provide any significant shielding from cross-talk. Finally, as with GaAs and HRS, the idea of shielding may be totally abandoned by making S_U very thick (for example 100–200 μm) and highly resistive. In this case, the dual resistivity substrate has no cross-talk advantage over GaAs or HRS, but it is still much easier and less expensive to make.

REFERENCES

[1] S. R. Taub and S. A. Alterovitz, "Silicon technologies adjust to RF applications," *Microwaves & RF*, pp. 60–74, Oct. 1994.

[2] A. K. Agarwal *et al.*, "MICROX—an advanced silicon technology from microwave circuits up to x-band," in *Proc. 1991 IEEE Int. Electron Devices Meeting*, pp. 687–690.

[3] T. M. Hyltin, "Microstrip transmission on semiconductor dielectrics," *IEEE Trans. Microwave Theory Tech.*, vol. MTT-13, no. 6, pp. 777–780, Nov. 1965.

[4] A. Rosen *et al.*, "Silicon as a millimeter-wave monolithically integrated substrate—a new look," *RCA Rev.*, vol. 42, pp. 633–660, 1981.

[5] S. R. Taub and P. Young, "Temperature dependent performance of coplanar waveguide (CPW) on substrates of various materials," *Proc. 1994 IEEE MTT-S Int. Microwave Symp.*, pp. 1049–1051, May 1994.

[6] *Atlas User's Manual*, 2nd ed., Silvaco International, Mar. 1, 1994.

[7] S. Wolf and R. N. Tauber, *Silicon Processing for the VLSI Era, Volume 1: Process Technology*. Sunset Beach, CA: Lattice, 1986, pp. 176–177.

Spectral Domain Analysis of Single and Coupled Microstrip Open Discontinuities with Anisotropic Substrates

Jaideva C. Goswami, Andrew K. Chan, and Charles K. Chui

Abstract— **The normalized input admittance for single and coupled microstrip open discontinuities with anisotropic substrates are obtained using a full-wave analysis. Problem is formulated in terms of the field Green's function in the spectral domain. Numerical results are found to be in good agreement with the published theoretical and experimental results for microstrip open discontinuities with anisotropic/isotropic substrates.**

I. INTRODUCTION

Extensive research related to discontinuities in planar transmission lines with isotropic substrates has been carried out. However, results for the propagation characteristics and discontinuity effects of transmission lines with anisotropic substrates are scant. In fact, there seems to be only one paper [1] that deals with microstrip open discontinuity on anisotropic substrates. In [1], a dynamic source reversal method based on potential theory has been used to compute open circuit capacitance. The microstrip is enclosed in a waveguide of infinite extent, operating in its cut-off mode.

The objective of this paper is to analyze the end effects of single and coupled microstrip open discontinuities with uniaxial substrates using spectral domain method. The analysis presented in the paper can be reduced to the isotropic case with some trivial modifications. Furthermore, it can be extended to slot line and CPW line by using appropriate Green's function. The paper is organized as follows. In the next section we discuss the formulation of the problem for coupled microstrip line which can be easily modified for single line. There are a couple of papers that deal with the Green's function in uniaxial medium. We avoid repeating the derivation by giving proper reference. The real-axis integration method is used to evaluate various integrals involved in the formulation. For this purpose, we provide the expressions for the asymptotic form, poles and residues of the Green's function in Sections II and III. In Section IV, we discuss the numerical results and compare them with the published ones. Finally, we conclude our work in Section V.

Manuscript received September 14, 1995; revised March 20, 1996. This work was supported in part by the Texas Higher Education Coordinating Board under Grants 999903-066 and 999903-067.

J. C. Goswami is with the Electromagnetic Communication Laboratory, University of Illinois at Urbana-Champaign, IL 61801 USA.

A. K. Chan is with the Electromagnetics and Microwave Laboratory, Department of Electrical Engineering, Texas A&M University, College Station, TX 77843-3128 USA.

C. K. Chui is with the Center for Approximation Theory, Department of Mathematics, Texas A&M University, College Station, TX 77843-3368 USA.

Publisher Item Identifier S 0018-9480(96)04727-8.

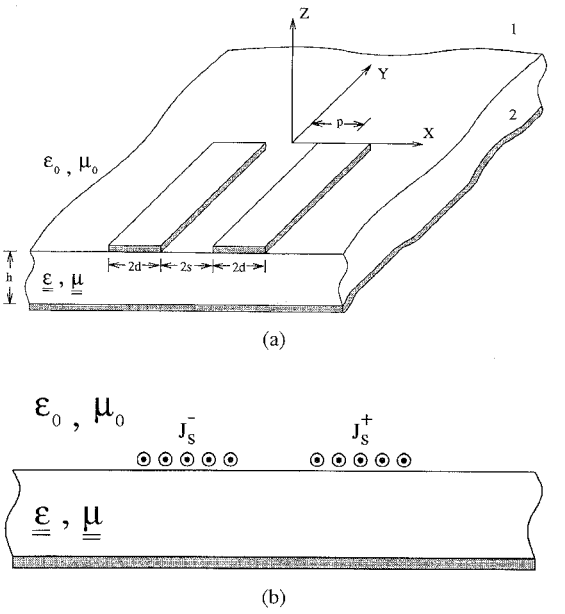


Fig. 1. (a) Open coupled-microstrip and (b) the equivalent problem.

II. FORMULATION

Transmission line configuration to be studied is shown in Fig. 1(a). We assume that the metal thickness is zero and that the substrate is lossless. Observe that the configuration shown in Fig. 1(a) reduces to that of a single microstrip line for $p = 0$.

We will use field integral equations in spectral domain for the purpose of analysis. Although we provide results for dielectric anisotropy only, let us, for a general case, consider that the substrate is characterized by both the relative permittivity and permeability tensors, given as

$$\underline{\underline{\epsilon}} = \underline{\underline{\mathbf{I}}}_t \epsilon_t + \hat{\mathbf{z}}\hat{\mathbf{z}}\epsilon_z, \quad \underline{\underline{\mu}} = \underline{\underline{\mathbf{I}}}_t \mu_t + \hat{\mathbf{z}}\hat{\mathbf{z}}\mu_z \tag{1}$$

where $\underline{\underline{\mathbf{I}}}_t$ is the identity dyadic, transverse to the optic axis $\hat{\mathbf{z}}$. Let the electric and magnetic anisotropy ratios ν^e and ν^h be defined as

$$\nu^e = \frac{\epsilon_t}{\epsilon_z}, \quad \nu^h = \frac{\mu_t}{\mu_z}. \tag{2}$$

For the medium characterized by (1), the time-harmonic form of the Maxwell's equation becomes

$$-\nabla \times \mathbf{E} = j\omega\mu_0 \underline{\underline{\mu}} \cdot \mathbf{H} + \mathbf{M} \tag{3}$$

$$\nabla \times \mathbf{H} = j\omega\epsilon_0 \underline{\underline{\epsilon}} \cdot \mathbf{E} + \mathbf{J}. \tag{4}$$

The dyadic electric field Green's function $\underline{\underline{\mathbf{G}}}^{EJ}(\mathbf{r}, \mathbf{r}')$ can be obtained from (3) and (4) in terms of the transmission line Green's function [2, Ch. 2]. A detail description of such formulation is given in [3].